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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/702,870	11/01/2000	Keiichi Den	ROH-030	9736

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EXAMINER
THAI, LUAN C

ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/702,870	Applicant(s) DEN, KEIICHI
	Examiner Luan Thai	Art Unit 2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5,7-10,12-20 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-5,7-10,12-20 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office action is responsive to the amendment filed March 19, 2002.

Claims **2-5, 7-10, 12-20,** and **22-25** are pending in this application.

Claims **1, 6, 11, and 21** have been canceled.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2, 4-5, 7-10, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. (5,821,625 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 7-10, and 22, Yoshida et al. (specifically see figures 3A-3E and 4A-4B) show a semiconductor device comprising: a first semiconductor chip 5; a second semiconductor chip 1 bonded onto the first semiconductor chip 1 in stacked relation, wherein chip 5 is greater in size than chip 1 (see figures 1, 3D, 3E); a noise shield film (7, 12) provided between the first and second semiconductor chips 5-1 for preventing the first and second chips from being mutually influenced by noises thereof (Col. 2, lines 24+, 38+, Col. 9, lines 47+).

The device package, as being shown in Yoshida et al.'s figures 3A-3E, does not disclose that the noise film 12 (or 7) is extended beyond an edge of the second chip 1. However, Yoshida et al. further teach that the noise shield film (7, 12) can be formed to cover entire surface of semiconductor chip 5, excluding electrode pads 6 (Col. 5, lines 63+), for simplifying the process of making the package (Col. 6, lines 1+), as being shown in Figure 4A-4B. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the process of forming the noise shield film covering entire surface of semiconductor chip 5, as being shown in Figure 4B, to the chip 5 of the device package shown in figures 3D-3E, in order to simplify the process of making the package. Because semiconductor chip 1, which bonds onto the chip 5, is smaller in size than chip 5 (see figures 1 and 3E), the noise shield film (7, 12) provided between the first chip 5 and second semiconductor chip 1, would be obviously extended outwardly beyond an edge of the second chip 1.

The proposed device package of Yoshida et al. discloses all the limitations of the claimed invention as detailed above except for teaching a major noise source being present in the second semiconductor chip 1. The claimed of the major noise source being present in the second semiconductor chip 1 is considered to be obvious over the proposed device of Yoshida et al. since Yoshida et al. do disclose that the noise shield film (7-12) is provided between the first and second semiconductor chips 5-1 for preventing the first and second

chips from being mutually influenced by noises thereof; thus, the noise source would be present in either chips 5-1 or both.

Regarding claim 2, although Yoshida et al. do not explicitly teach a connection mechanism which connects the noise shield film to a power supply portion, this feature (the connection mechanism) is seen to be an inherent teaching of Yoshida et al.'s device since a means for providing ground source for the noise shield film (7, 12) is disclosed (figures 2, 3A, 3D, 4B, 6, and Col. 4, lines 46+) and it is apparent that some type of connection mechanism must be present and connected between the noise shield film and the ground source for the noise shield film to function as intended.

Regarding claims 4-5, Yoshida et al. further disclose chip 1 and chip 5 being electrically connected via bump 4, wherein bump 4 is composed of the same material as the noise shield film (Col. 5, lines 58+, Col. 6, lines 8+).

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. (5,821,625 of record) in view of Fujimoto et al. (5,930,599 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 3, the proposed device package of Yoshida et al. discloses all the limitations of the claimed invention as detailed above except for the connection structure of the device and the lead frame. However, Yoshida et

al. do suggest that the device package may comprise a lead frame (Col. 4, lines 42+).

Fujimoto et al. (Figures 1-10) while relate to a similar semiconductor package design teach a device of a stacked chip die bonded to a lead frame with plurality of lead fingers 32-132 wire bonded 33-133 to the device for providing external terminals for the device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the lead frame as taught by Fujimoto et al. to the proposed device of Yoshida et al. in order to provide the external terminals for the device including a power source, a ground potential, and in/out signal.

4. Claims 12-16, 19-20 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohki et al. (5,886,408).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 13-14, 16, and 23, Ohki et al. (see specifically figures 12-25) a semiconductor device comprising a first chip 232-3; a second chip 232-1 bonded onto the first chip in stacked relation; a heat conductive member 240 provided between the first and the second chips to define a heat release path for releasing heat generated by the chips; a connection member 234 (e.g., conductive block) thermally connecting the heat conductive member 240 to a heat sink 236, wherein the heat conductive member 240 includes a first metal

film 242 provided on a surface of the first semiconductor chip 232-3 and a second metal film 241 provided on a surface of the second chip 232-1, and the first metal film and the second metal film are disposed in contact with each other via conductive member 240. Although Ohki et al. do not label the conductive block 234 to be "a bonding wire" as Applicant's claimed, the conductive block 234 performs the same function as that of the claimed "bonding wire", that is "thermally connecting the heat conductive member to a heat sink" (see figures 14, 23, 25), and the device package disclosed by Ohki et al. in figure 12 does not distinguish from the claimed structure. Further, the labels nonetheless are meaningless. The Ohki et al.'s structure anticipates Applicant's claimed structure regardless of whether the layer is labeled "bonding wire". See *In re Pearson*, 181 USPQ 642; Fx parte Minks 169 USPQ 120; or *In re* Swinehart 169 USPQ 226, all of which make it clear that mere "labels" or "statements of in intended use" as we have here in "bonding wire" do not distinguish over Ohki et al.'s structure which may be likewise labeled.

Regarding claims 12, 15, and 24, Ohki et al. (see specifically figures 12-25) a semiconductor device comprising a first chip 232-1; a second chip 232-3 bonded onto the first chip in stacked relation, wherein the first chip 232-1 is greater in size than the second chip 232-3 (figure 12); a heat conductive member 240 provided between the first and the second chips to define a heat release path for releasing heat generated by the chips; a connection member 234 (e.g., conductive block) thermally connecting the heat conductive member 240 to a

heat sink 236, wherein the heat conductive member 240 includes a first thin film wiring layer 241 provided on a surface of the first semiconductor chip 232-1 and a second thin film wiring layer 242 provided on a surface of the second chip 232-3, and the first thin film wiring layer and the second thin film wiring layer are disposed in contact with each other via conductive member 240. Although Ohki et al. do not explicitly teach the thin film wiring layer 242 being thermally connected to the heat radiator via the connection member, this feature is taken to be inherent in Ohki et al.'s device, since the thin film wiring layer 242 is the only element to connected the chip (e.g., heat source) to the heat conductive member 240 (see figure 14) and it apparent that a heat path must exist between the chip and the thin film wiring layer 242 and between the thin film wiring layer 242 and the heat conductive member 240. Ohki et al. do not explicitly teach a metal film provided on a surface of at least one of the first chip and the second chip.

Ohki et al. disclose element 242 (or 241) as a "thin film-wiring layer" and a wiring layer is well known in the art for being made of metal (e.g., copper, aluminum, gold, silver, etc.). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the thin film wiring layer comprising a metal wiring layer since metal is conventional in semiconductor art for forming a wiring layer.

Regarding claim 19, Ohki et al. further disclose the first chip 232-3 bonded to the conductive member 240, which would be obviously to be considered as the mounting pad of the lead frame 237.

Regarding claim 20, Ohki et al. further disclose the first and the second semiconductor chips can be boned to each other with active surfaces thereof being opposed to each other (see figures 19-21).

5. Claims 17-18 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohki et al. (5,886,408) in view of Byun (5,668,040).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 17-18 and 25, the proposed device package of Ohki et al. discloses all the limitations of the claimed invention (including electrodes formed on chip 232-1 and 232-3 for electrically connected to the bums 245 and to wires 246 respectively) as detailed above except for teaching the metal film composed of the same material as the electrode portion.

Byun teaches copper is a well-known material for making wiring layer and electrode (Col. 1, lines 29+ and lines 49+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use copper for forming electrodes and metal wiring layer in the proposed device of Ohki et al. since copper is a conventional material in semiconductor art as taught by Byun.

Conclusion

6. Applicant's arguments with respect to claims **2-5, 7-10, 12-20,** and **22-25** have been fully considered, but they are deemed to be moot in view of the new grounds of rejection.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action because the change (e.g., underlined portions) in claims 2, 4, 7-10, 12-17, 19-20, and 22-25 raise new issues that would require further consideration and/or search. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211. The examiner can normally be reached on 7:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Luan Thai
May 29, 2002

DAVID L. TALBOTT
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